Reduction of BER in the physical Layer of OFDMA

Dr. Salauddin Mohommad[1], Dr. Abhinav Sharma[2]
Electronics, Instrumentation & Control Dept. UPES, Dehradun[1, 2]

Abstract:IEEE 802.16 standard which works for the mobile broad band services is one of the emerging technologies worldwide. There is a need of achieving high data rate to compensate the requirements and the applications. The high speed depends on how fast and how efficient the data is received by the receiver when transmitted from the transmitter. Since the signal which is a group of symbols travel to the receiver via multiple paths and hence there is a high chance of Inter symbol Interference (ISI) especially in the high data rate applications. And it is even more when the receiver is in moving condition. So, there is a need to reduce the ISI and the multipath fading of the signal for the applications mentioned. Bit Error Rate (BER) of LMS, RLS and CMA Equalizer algorithms are studied in the literature review to reduce the ISI [1] for IEEE 802.16e standard i.e. Orthogonal Frequency Division Multiple Access(OFDMA).Apart from equalization algorithms Fast Fourier Transform (FFT) window, which is important aspect of physical layer of OFDMA can be positioned at the downlink module of OFDMA system ensuring all the symbols have been received at the receiver to reduce the interference and increase the SNR. Xilinx ISE 14.2 andModelsim 10.2 have been used to simulate and compare the results and Vertex-5 FPGA for Synthesis. The results of the proposed method show 4.8% significant improvement of SNR.
Keywords: OFDMA, FFT, Equalization algorithms, signal Interference.

I Introduction

The IEEE 802.16 is a series of wireless broad band standards which was proposed in the year 2005. Apart from Frequency Division Multiplexing (FDM) and Orthogonal Frequency Division Multiplexing (OFDM), OFDMA was deployed in the current standard. The only difference between the OFDM and OFDMA is the capacity of handling the users end also efficiently. The OFDM is a fixed standard i.e 256-pt FFT at a particular given time and OFDMA[2] is scalable i.e. it can handle either 128-pt FFT, 512-pt FFT, 1024-pt FFT and 2048-pt FFT depending on the users number of users using the channel[3].In the high data rate application the signal can be faded easily which is actually classified into two type namely narrow band and wide band fading. And also the multipath fading causes the ISI. Many algorithms like Least Mean Square LMS, Recursive Least square (RLS) and Constant Modulus Algorithm (CMA) have been applied at the down link module of the receiver side to minimize the ISI caused by multipath fading [4]. Apart from these, 2D-MMSE (Minimum Mean Square Error) is also proposed. However, in the most practical wireless systems it is not so easy to design the 2D-MMSE equalizer [5]. Hence we propose a new technique for the mitigation of ISI in which the delay spread will be calculated and the FFT window will be positioned according to the delay. The Mean excess delay and the RMS delay spread are used to calculate the delay time of

the symbols. The delay can be produced by using the farrow filters which provide the fractional delay[6].

The rest of the paper is organized as follows: in section II we introduce the system model of the OFDMA system along with the delay calculations. Section III gives the proposed positioning of the FFT window system followed by the section IV to show the simulation results and the comparisons of simulated results on the Xilinx ISE and Vertex-5 FPGA and the last section concludes the chapter.

II Modelling of OFDMA system

The OFDMA technology works by splitting the radio signal into multiple smaller sub-signals that are then transmitted simultaneously at different frequencies to the receiver.

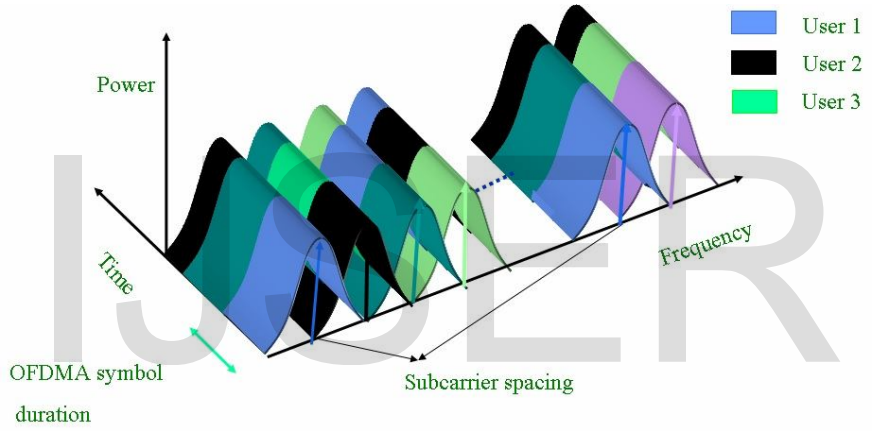


Fig.1. Orthogonal Frequency Division Multiple Access signal

The serial data is converted to parallel data and digital modulation scheme like M-PSK or M-QAM is applied to form the symbols and process the Inverse Fast Fourier Transform (IFFT). Cyclic prefix is added at the end of the each symbol to indicate the end of each symbol at the receiver and hence the OFDM/A symbols are obtained which is to be transmitted into the channel. At the receiver point of view both the OFDM and SOFDMA techniques are same since at an instance of given time OFDM performs fixed point FFT i.e. 256-pt FFT and OFDMA can perform variable length FFT.

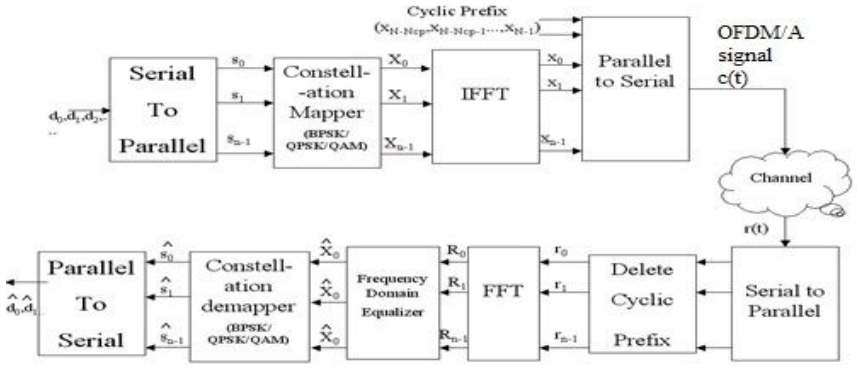


Fig.2. OFDMA communication Architecture with Cyclic Prefix

Usually QAM-64 is used for high data rate applications like DVB-T and DVB-H systems. The each symbol is prefixed by a Cyclic Prefix (CP) [7] in order to overcome the interference caused the symbols during transmission in the channel. For an optimum case the cyclic prefix must be kept at least four times larger than the expected delay spread. The output of the IFFT in the time domain can be given as in equation.1.

$$X_k(n) = \frac{1}{\sqrt{N}} \sum_{i=0}^{N-1} X_m(i)\, e^{j 2\Pi \frac{n}{N} i} \quad (1)$$

Where $0 \le i \le N\text{-}1$; $0 \le n \le N\text{-}1$

Where $X_k(n)$ and $X_m(i)$ represents the sequence in time and frequency domains. Similarly the output of the Fast Fourier transform in the frequency domain can be given as in equation.2.

$$R_{m(i)} = \sum_{n=0}^{N-1} r_{k(n)} e^{-j 2\Pi \frac{n}{N} i} \quad (2)$$

2D-FFT algorithm is used in the implementation of the FFT processor for OFDMA system and this FFT processing will be delayed with respect to the delay. The flow chart of the implementation is shown in Fig.3.

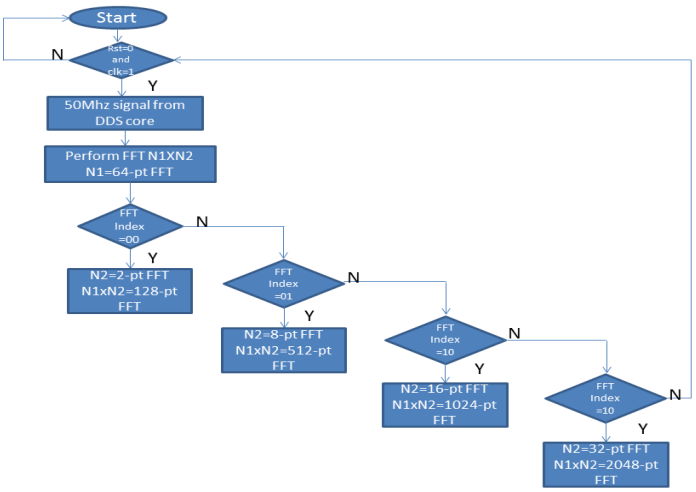


Fig.3. Flowchart of 2D-FFT algorithm implementation for OFDMA

The output of the FFT is fed to appropriate equalizer whose impulse response is the inverse of the channel response for the reduction of ISI. The BER of the various equalizer algorithms [8] with different modulation schemes is shown in the Table.1.

Table.1. BER of LMS, RLS and CMA Equalizer for OFDM/A System

Equalization	BER of OFDM/A based BPSK system	BER of OFDM/A based QPSK system	BER of OFDM/A based QAM system
LMS	0.845	0.909	0.874
RLS	0.848	0.878	0.938
CMA	0.818	0.939	0.874

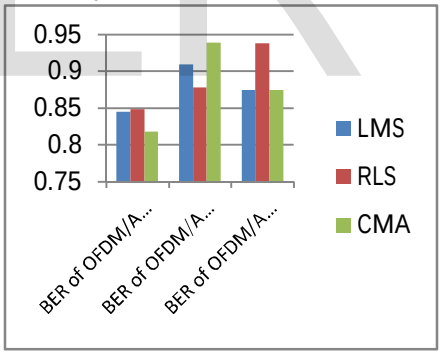


Fig.4.BER of LMS, RLS and CMA Equalizer for OFDM/A System

III Proposed system

At the downlink module of OFDMA, the delay needs to be calculated before the FFT processing is started. For this we must ensure that all the symbols have been arrived at the input of the receiver.

This is done by calculating the RMS delay spread and then giving that each symbol to the fractional delay filters which provides fractional delay and minimizes the ISI.

The Mean excess delay and the RMS delay spread are used to calculate the delay time of the symbols. The Mean excess delayis given as

$$\overline{\tau} = \frac{\sum_k P(\tau_k)\tau_k}{\sum_k P(\tau_k)} \tag{3}$$

Where $\overline{\tau}$ is the RMS delay spread, $P(\tau_k)$ is the absolute power of the received signal and delay of the k[th] detectable signal arriving at the receiver is denoted by $P(\tau_k)$.

The RMS delay spread can be derived from the mean excess delay as shown in equation 4.

$$\sigma_\tau = \sqrt{\overline{\tau^2} - \overline{\tau}^2} \tag{4}$$

The RMS delay is also useful to estimate the type of the interference based on the coherence bandwidth. Coherence bandwidth is less than the signal bandwidth in the frequency selective fading. The relation between the RMS delay spread and coherence bandwidth is given as

$$B_C \approx \frac{1}{5\sigma_\tau} \tag{5}$$

Based on the delay the FFT window is shifted by passing the signal through a Farrow filter which is also known as fractional delay filters.

IV Simulation Results

The simulations have been carried out by considering different test cases and different delays. The delays shown in the result are with delay 0 µs, 0.41 µs, 2.41 µs. Fig.5. shows the RTL view of the FFT Processor

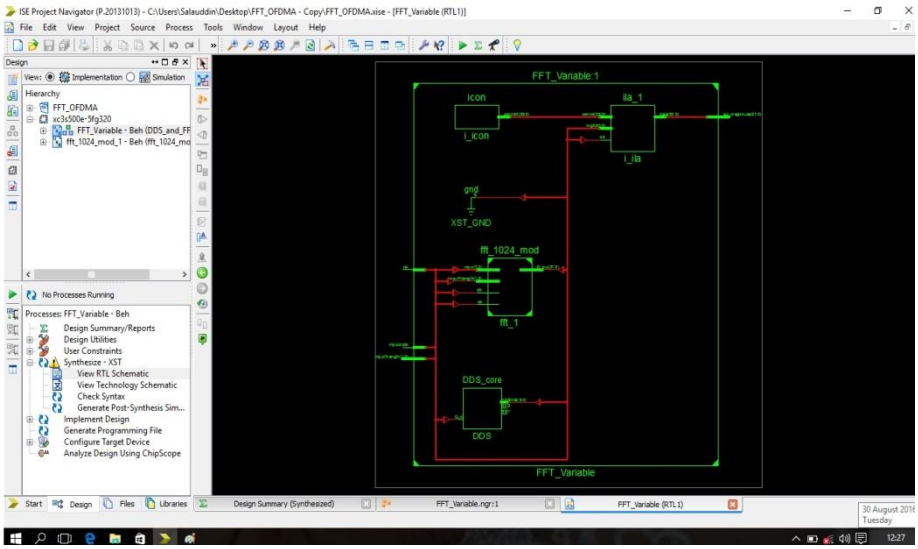
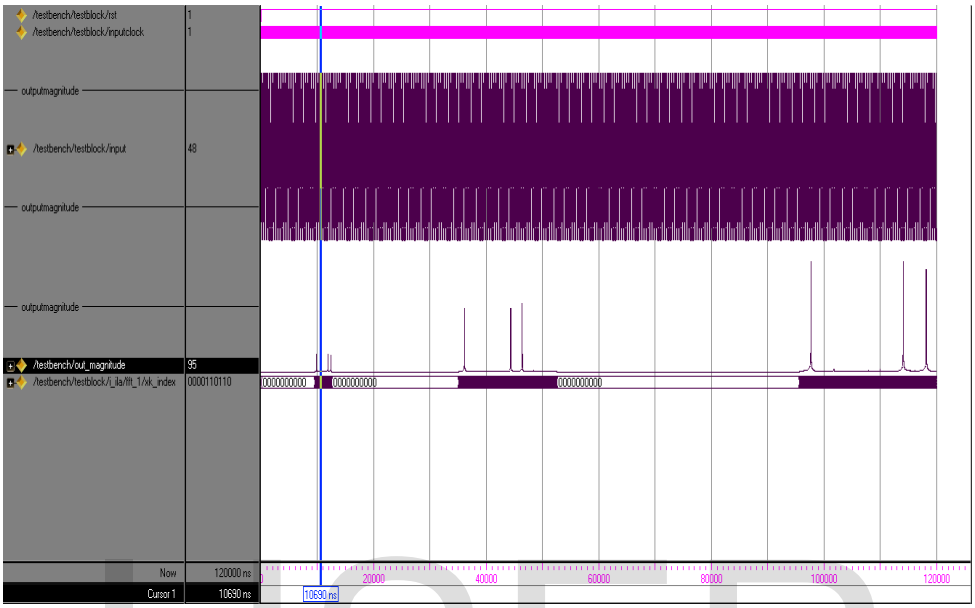


Fig.5. RTL View of variable length FFT processor

Test cases of functional simulation

I) Ideal Test Case: In thisTest case the delay is considered as zero and depending on the FFT index the FFT point is chosen and the output is shown in Fig.6. The time taken to calculate the same are given in the Table 2. Similarly the other test cases are shown in Table 3 and Table 4.

Delay =0 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	7.37 µs	7.370µs
01	512-pt FFT	9.945 µs	33.653 µs	23.708 µs
10	1024-pt FFT	43.909 µs	95.166 µs	51.257 µs
11	2048-pt FFT	111.56 µs	216.344µs	104.78 µs



II) Pedestrian Test Case: Delay=0.41 µs

Delay =0.41 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	7.78 µs	7.78µs
01	512-pt FFT	10.355 µs	34.065 µs	23.710 µs
10	1024-pt FFT	44.323 µs	95.576 µs	51.253 µs
11	2048-pt FFT	111.944 µs	216.754µs	104.81 µs

III) Vehicular Test Case: Delay=2.51 µs

Delay =2.51 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	9.88 µs	9.88 µs

01	512-pt FFT	12.455 µs	36.173 µs	23.718 µs
10	1024-pt FFT	46.419 µs	97.676 µs	51.257 µs
11	2048-pt FFT	114.052 µs	218.854µs	104.802 µs

The same test cases have been carried out for synthesis verification on Vertex-5 FPGA hardware and the results shown are matched with some hardware delay to process the long FFT's. the hardware utilization report is shown in the Table 5.

Device utilization summary

Table 5 Device utilization summary

Device utilization summary
Selected Device : 5vfx130tff1738-2
Slice Logic Utilization
Number of Slice Registers : 5700 out of 81920 6%
Number of Slice LUTs: 10865 out of 81920 13%
Number used as Logic: 10865 out of 81920 13%
Slice Logic Distribution
Number of LUT Flip Flop pairs used: 14267
Number with an unused Flip Flop: 8567 out of 14267 60%
Number with an unused LUT: 3402 out of 14267 23%
Number of fully used LUT-FF pairs: 2298 out of 14267 16%
Number of unique control sets: 37

IO Utilization				
Number of IOs:	32			
Number of bonded IOBs:	32	out of	840	3%
Specific Feature Utilization				
Number of BUFG/BUFGCTRLs:	4	out of	32	12%
Number of DSP48Es:	134	out of	320	41%

Conclusion:

The paper gives the following conclusions: In the high data rate applications like DVB-H and DVB-T, the ISI is an important parameter to consider and the signal interference is mitigated by positioning the FFT window in the case of interference. The results show the improvement of SNR by 4.8% for the proposed system over conventional OFDMA system. Hence the same system can be used for the real time applications and super imposed training sequence of symbols can be done to the same system do avoid cyclic prefix and utilize the bandwidth more efficiently.

VI References

[1] Markus Rupp,"Convergence Properties of Adaptive Equalizer Algorithms" in IEEE Transactions on signal processing, VOL. 59, No. 6, june 2011.

[2] E. Hari Krishna, K. Sivani, K. Ashoka Reddy, "Hardware implementation of OFDM transceiver using FPGA" in International Conference onComputer and Computational Sciences (ICCCS), 2015

[3] Chung-Ping Hung, Sau-Gee Chen and Kun-Lung Chen, "Design Of an Efficient Variable Length FFT Processor "in IEEE International Symposium on Circuits and Systems.2004.

[4] Van Duc Nguyen, H.P. Kuchenbecker, "Intercarrier and inter symbol interference analysis of OFDM systems on time-varying channels" 4th IEEE Workshop on signal processing Advances in Wireless Communications, 2003.

[5] Yang yang Fan, Xue Chen, Weiqin Zhou, Xian Zhou, Hai Zhu, "The Comparison of CMA and LMS Equalization Algorithms in Optical Coherent Receivers" in 6th International Conference

onWireless Communications Networking and Mobile Computing (WiCOM)-Electronic ISBN: 978-1-4244-3707-8

[6] Yao Liang, Weiou Zhou, Mingyu Zhou, Li He, "Research and implementation for 2D MMSE channel estimation" 12th International Conference on Signal Processing (ICSP)-10.1109/ICOSP.2014.7015267

[7] Wei-Chang Chen, Char-Dir Chung, "Spectral Precoding for Cyclic-Prefixed OFDMA with Interleaved Subcarrier Allocation" in IEEE transactions on communications, vol. 61, No 11, Nov. 2013.

[8] Jeffrey G. Andrews, Arunabha Ghosh, Rias Muhamed, Fundamentals of WiMAX: Understanding Broadband wireless Networking, Prentice Hall, 2007.